



IEEE Symposium on Low-Power and High-Speed Chips

# COOL Chips 20

Yokohama Joho Bunka Center, Yokohama, Japan  
(Yokohama Media & Communications Center)

April 19-21, 2017

## Panel Discussion

Topics: “Cool chips for the next decade”

## Yoshiaki Hagiwara

<http://www.aiplab.com/>  
Hagiwara-yoshiaki@aiplab.com

ISSCC® 2013 | February 17-21

## 60 Years of (Em)Powering the Future



### Plenary Talks (Monday, February 18)



Lisa Su  
Senior Vice President and  
General Manager, AMD  
Architecting the Future through  
Heterogeneous Computing



Martin van den Brink  
Executive Vice President and Chief  
Product & Technology Officer, ASML  
Next Generation Lithography:  
Progress and Outlook



Yoshiyuki Miyake  
Managing Director and  
CEO, Renesas  
Smart Life Solutions Group  
Home in Cities



Carver Mead  
Professor Emeritus, Caltech  
The Evolution of Technology

### 60th Anniversary Distinguished Evening Panel (Monday, February 18) "Antiques from the Innovations Attic"



Robert Briere  
Professor Emeritus,  
University of California,  
Berkeley



Rinaldo Schirru Gentile  
Professor  
University of Pavia



Yoshikazu Tanemoto  
Professor  
Soh University



Thomas Lee  
Director  
Microsystems Technology  
Office, DARPA



Nicky Lo  
Chairman  
Renesas Technology



Eric Veltz  
Independent Consultant

International Solid-State Circuits Conference  
February 17-21, 2013 | San Francisco, CA



Welcome to the 2013 IEEE International Solid-State Circuits Conference (ISSCC).

This year, we will celebrate the 60th anniversary of ISSCC. ISSCC is the flagship conference of the Solid-State Circuits Society, and is the premier forum for the presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity to network with leading experts in the field. For 2013, the Conference theme is “60 Years of (Em)Powering the Future”, more.



### Yoshiaki Higihara: The p-n-p-n Diode in Future Linear Motor Cars and in Modern Imagers

John Louis Moll (1921–2011) was studying a p-n-p-n diode switch in his Ph.D. dissertation work when the first ISSCC was held in 1954. In a normal operation mode, this device works as a thyristor, which can drive a large current and is the key device structure of an IGBT applied for a linear motor car of the future (see Figure 9). In a dynamic operation mode, this device may work as a simple p-n-p-n dynamic capacitance that can detect and store one single electron, which is a key device structure of the modern image sensor (see Figure 10).

I recall, when I was taking his physics course at Caltech, that Feynman once said that an electron is always free, moving around rapidly in free space, even in solid, and it

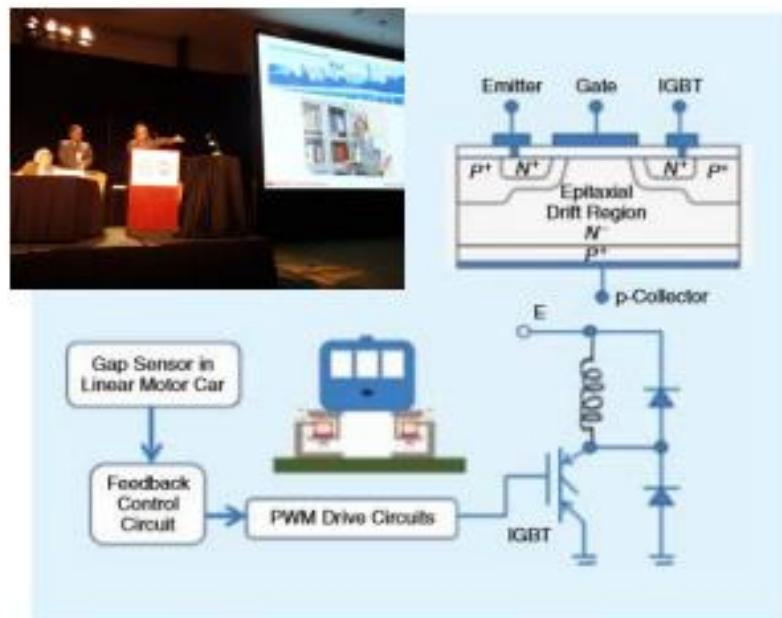


FIGURE 9: The p-n-p-n switch diodes for a modern linear motor car.



Yoshiaki Higihara, Eric Vittoz and Bob Brodersen never stops. It is very hard to catch an electron because we do not know exactly where it is. Our civilization today is based on a technology that controls electrons, down to a single one.

Imagine a photon incident to a bipolar transistor base region. The photon energy creates an electron-hole pair. And the photo-electron can be stored in the base region as one single majority carrier. That is, a bipolar transistor can also function as a photon detector and/or a storage container. I thought that a room in a hotel must be empty and clean before the first hotel guest arrives. So must be this transistor base region empty and clean with no guest electrons at the beginning. This transistor in a dynamic p-n-p mode is useful since it can capture, confine, and control one single electron. But as a

Yoshiaki Higihara shared his memories of Richard Feynman, his mentor and educator at Caltech, and how he learned from him that control of electrons is at the heart of all electronic devices. As an example from his attic, he pointed to the old p-n-p-n junctions that are now incorporated in modern-day image sensors.

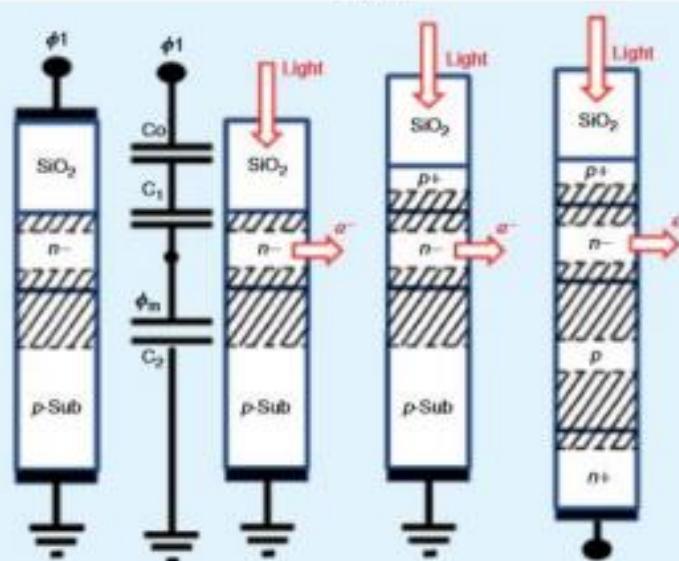
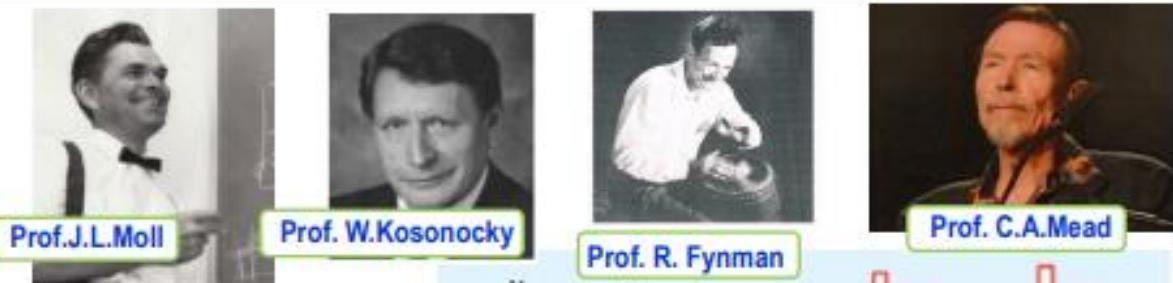


FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.



student, I did not know yet how to move that single photoelectron sitting in the base region to the outside world so that we can make use of it as a signal. I had no way yet to know whether the hotel guest has arrived and is resting in the hotel room or not. We had no way yet to ask the hotel guest to come up to the hotel lobby to meet me. I had to wait a few more years (until 1970 in my senior year in college) to find the answer. We all know now it is the CCD structure that can store and transfer one single electron. With a precharge reset set gate and a source-follower circuit, a scheme invented by Walter Kossenocky. We could finally meet our hotel guest at the hotel lobby.

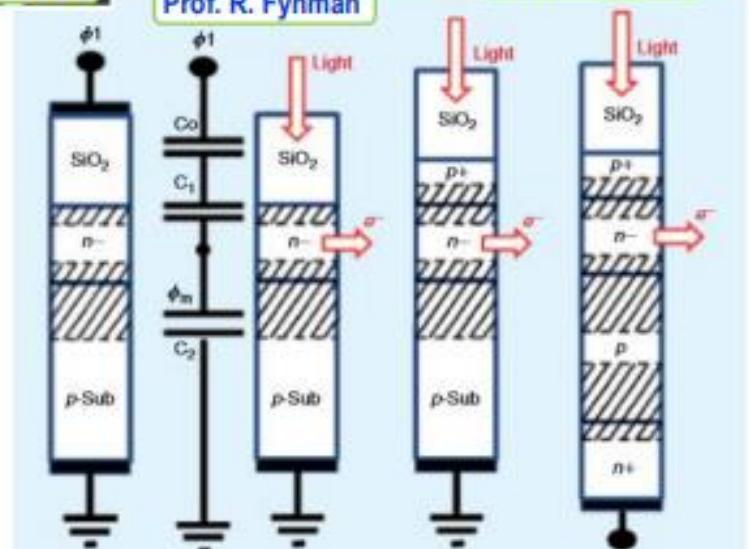


FIGURE 10: From CCD to the dynamic p-n-p-n diode capacitors.

## ISSCC 2017 / SESSION 4 / IMAGERS / 4.9

### 4.9 A 1ms High-Speed Vision Chip with 3D-Stacked 140GOPS Column-Parallel PEs for Spatio-Temporal Image Processing

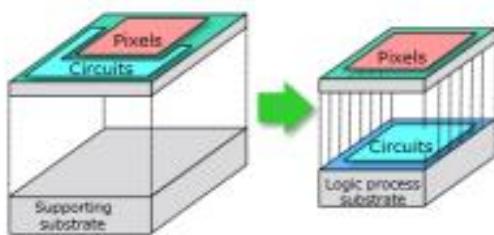
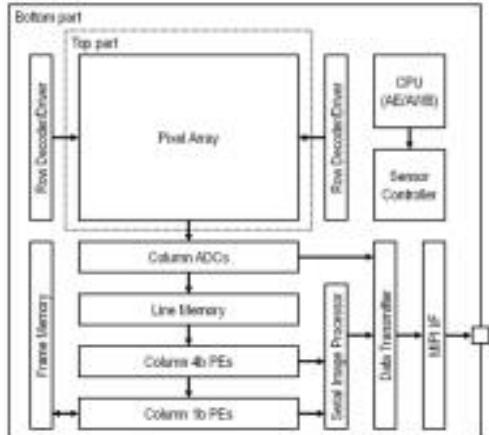
Tomohiro Yamazaki<sup>1</sup>, Hironobu Katayama<sup>1</sup>, Shuji Uehara<sup>1</sup>, Atsushi Nose<sup>1</sup>, Masatsugu Kobayashi<sup>1</sup>, Sayaka Shida<sup>1</sup>, Masaki Odahara<sup>1</sup>, Kenichi Takamiya<sup>2</sup>, Yasuaki Hisamatsu<sup>2</sup>, Shizunori Matsumoto<sup>2</sup>, Leo Miyashita<sup>2</sup>, Yoshihiro Watanabe<sup>2</sup>, Takashi Izawa<sup>2</sup>, Yoshinori Muramatsu<sup>2</sup>, Masatoshi Ishikawa<sup>2</sup>

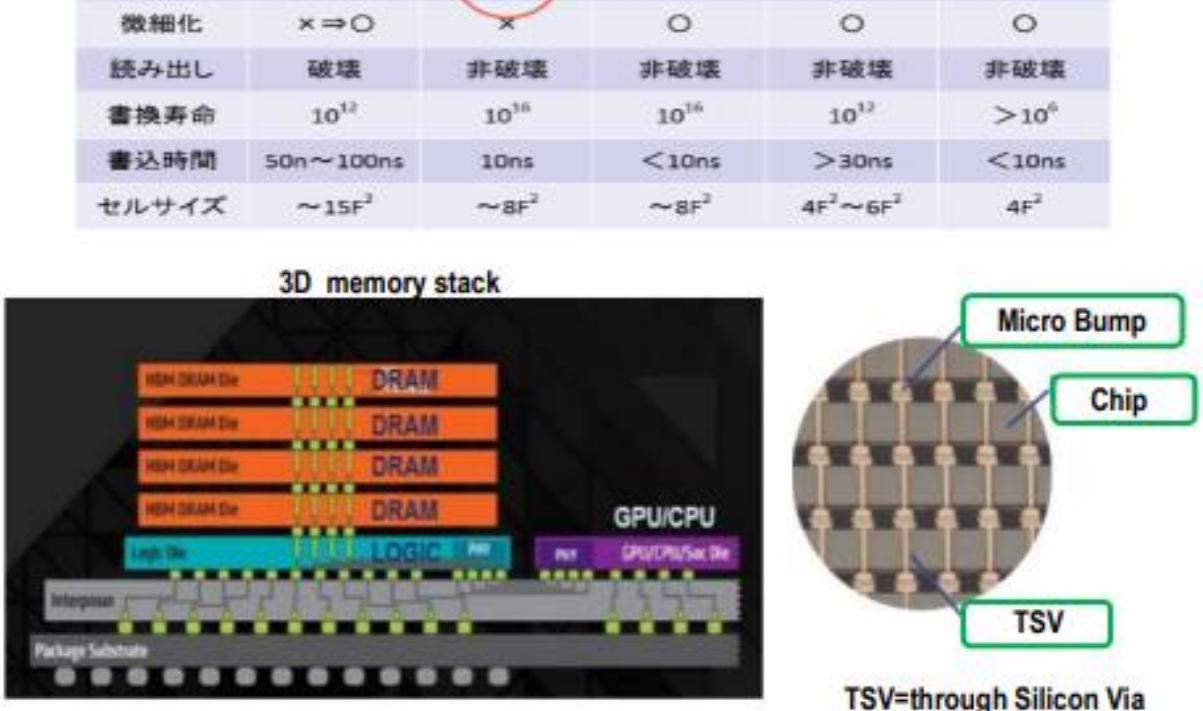
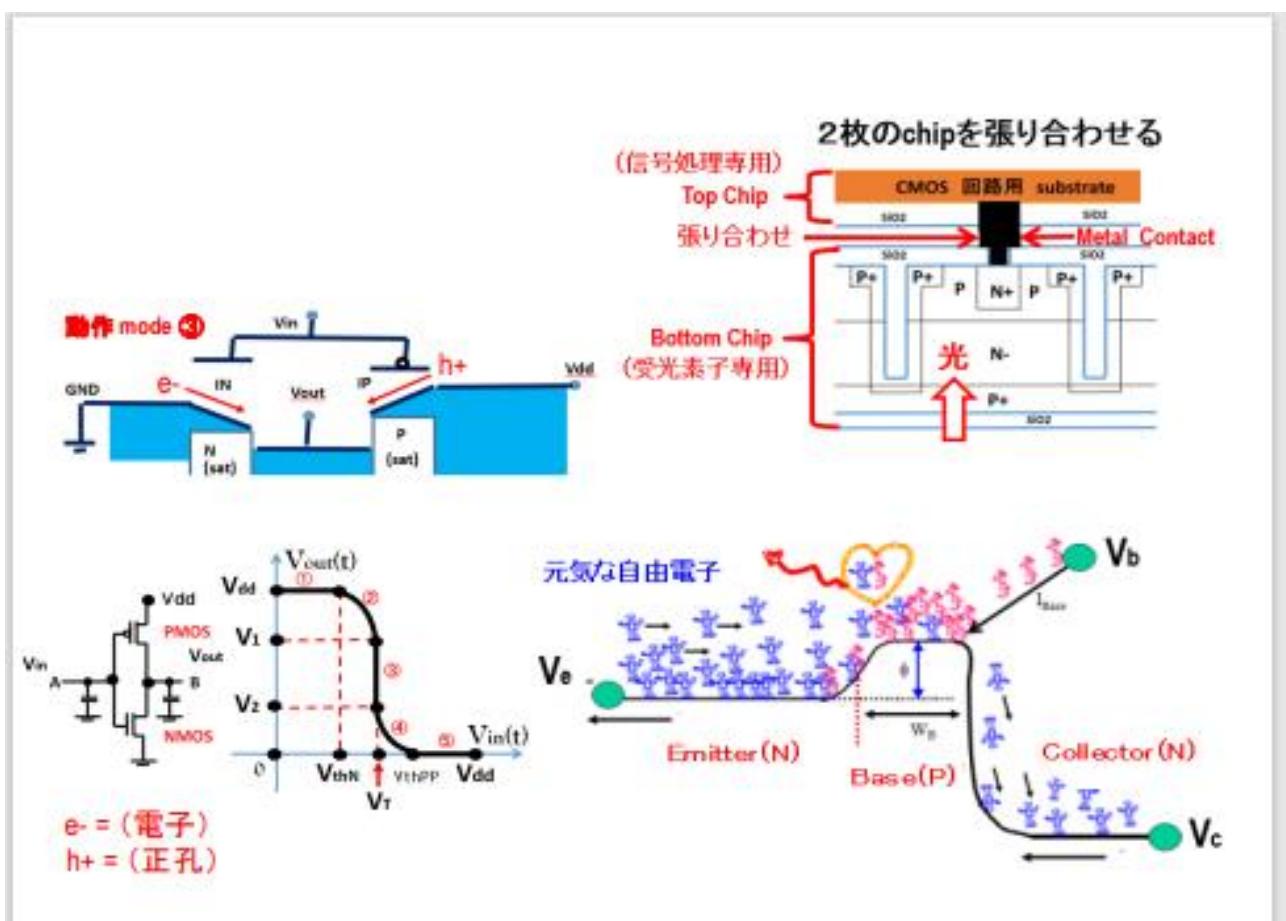
<sup>1</sup>Sony Semiconductor Solutions, Atsugi, Japan

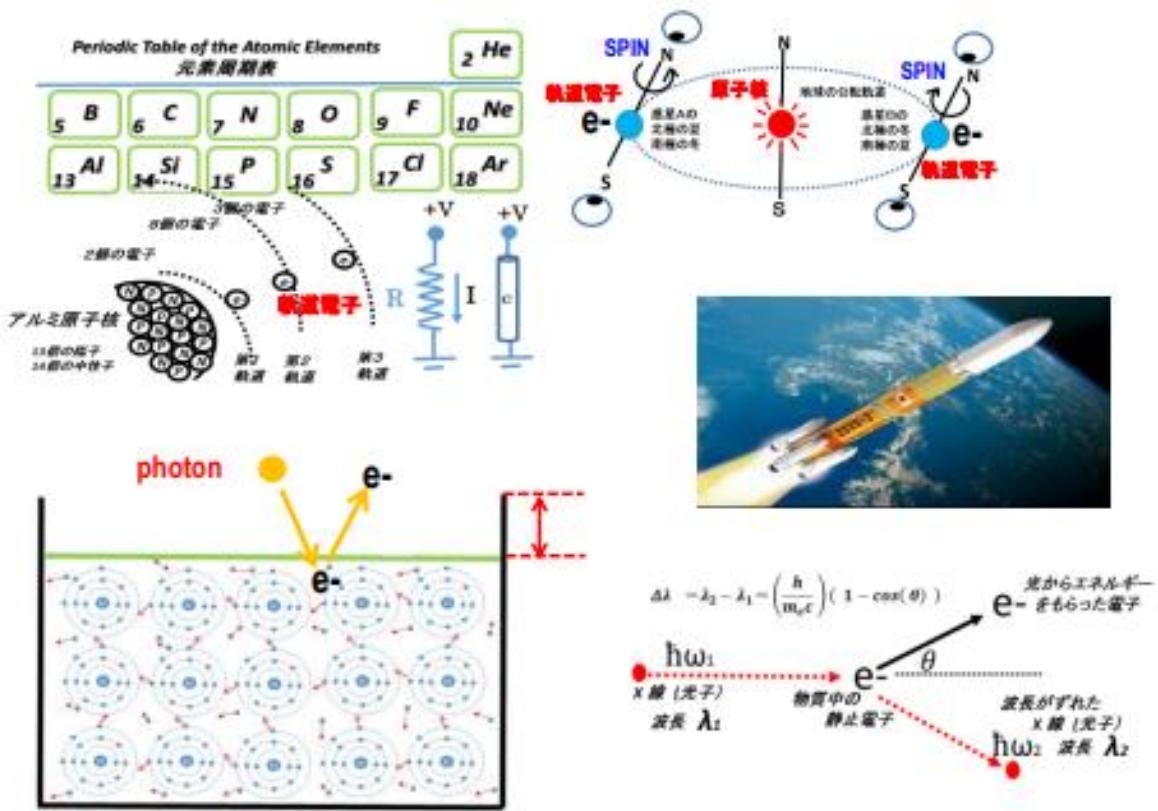
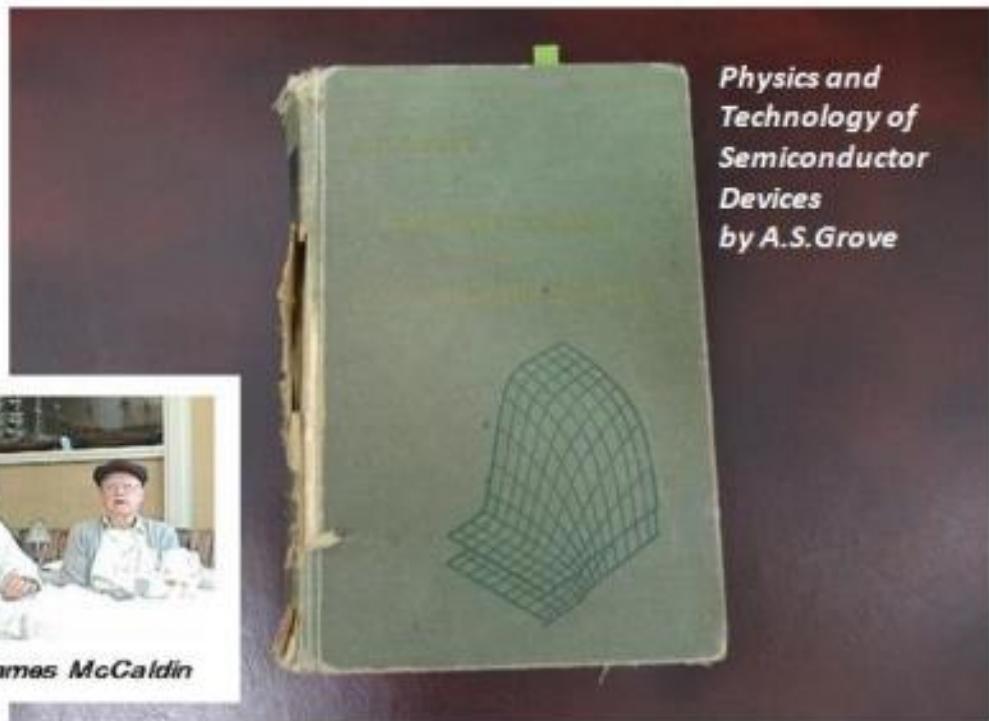
<sup>2</sup>Sony LSI Design, Atsugi, Japan

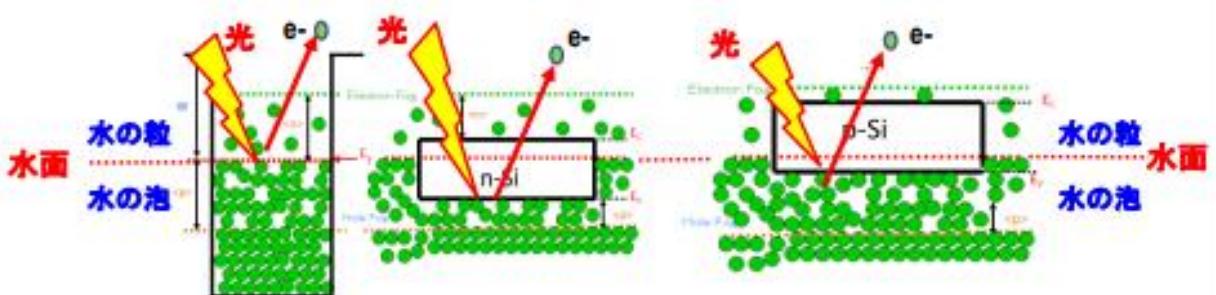
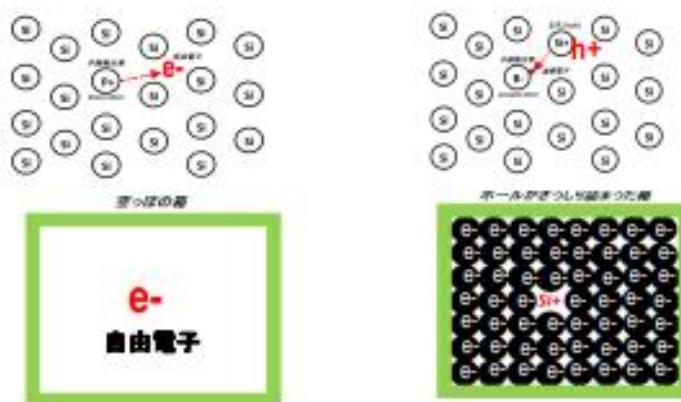
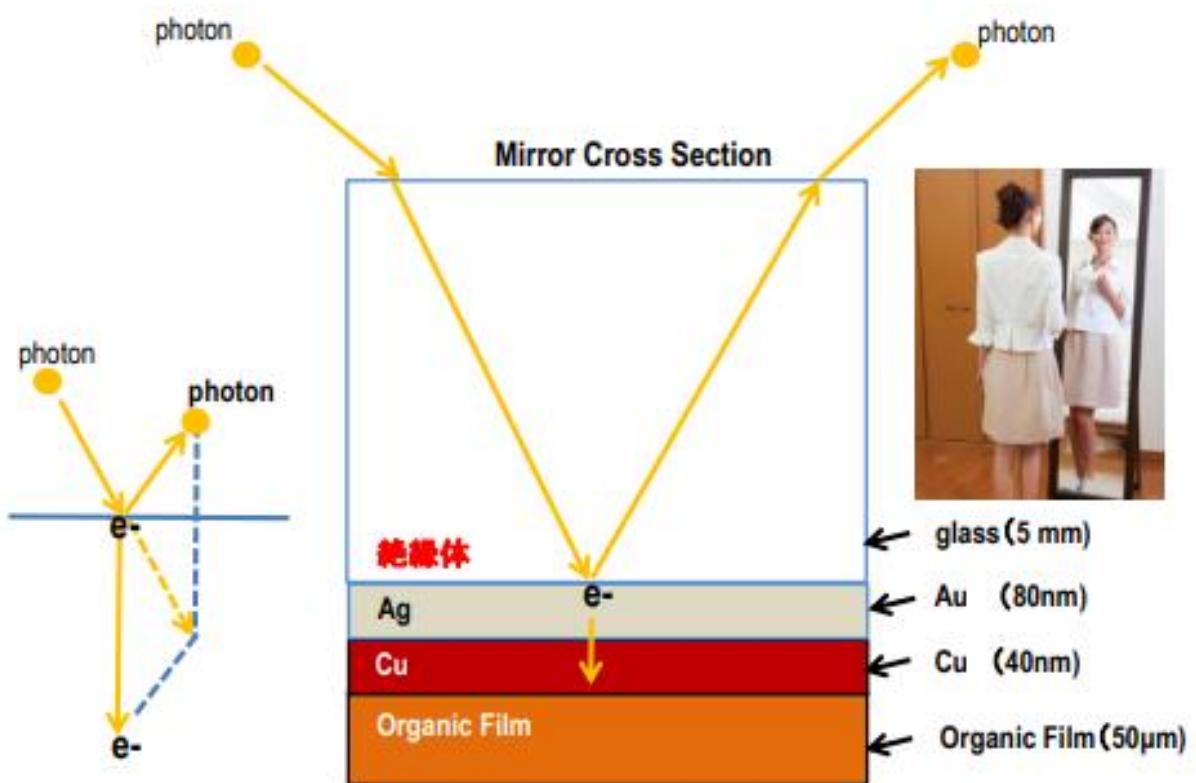
<sup>3</sup>University of Tokyo, Bunkyo, Japan

High-speed vision systems that combine high-frame-rate imaging and highly parallel signal processing enable instantaneous visual feedback to rapidly control machines over human-visual-recognition speeds.

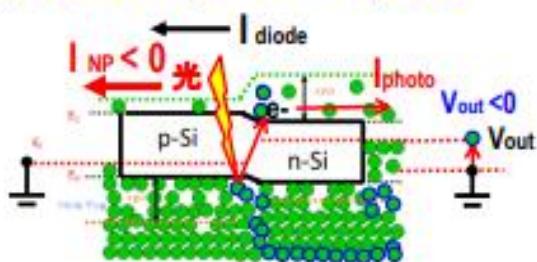




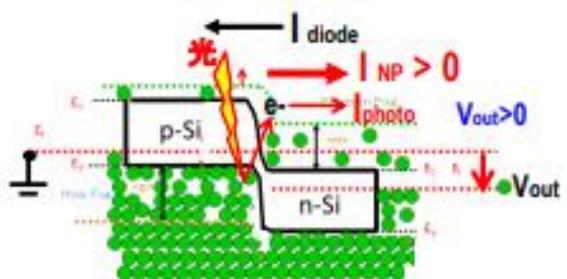




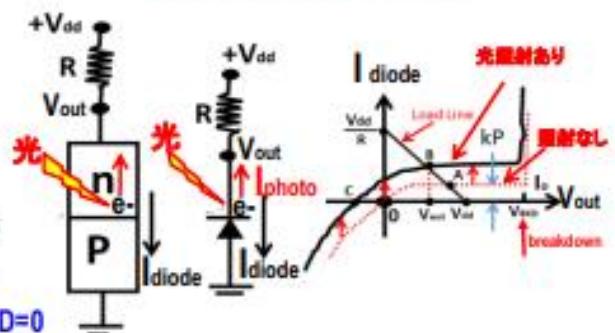
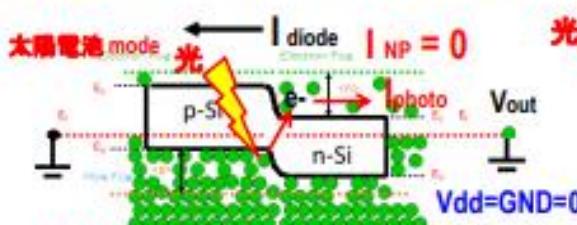
(1) 電源電圧  $V_{dd} < 0$  (遮断バイアス mode) の場合



(3) 電源電圧  $V_{dd} > 0$  (逆バイアス mode) の場合



(2) 電源電圧  $V_{dd} = GND = 0$  (NOバイアス mode) の場合



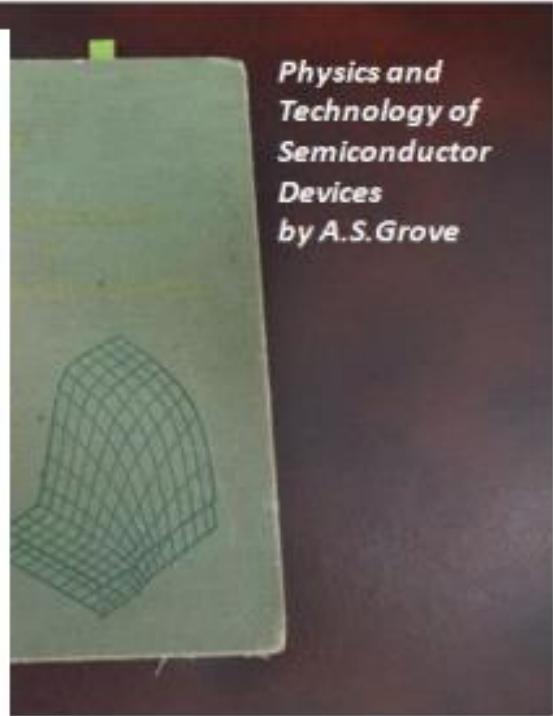
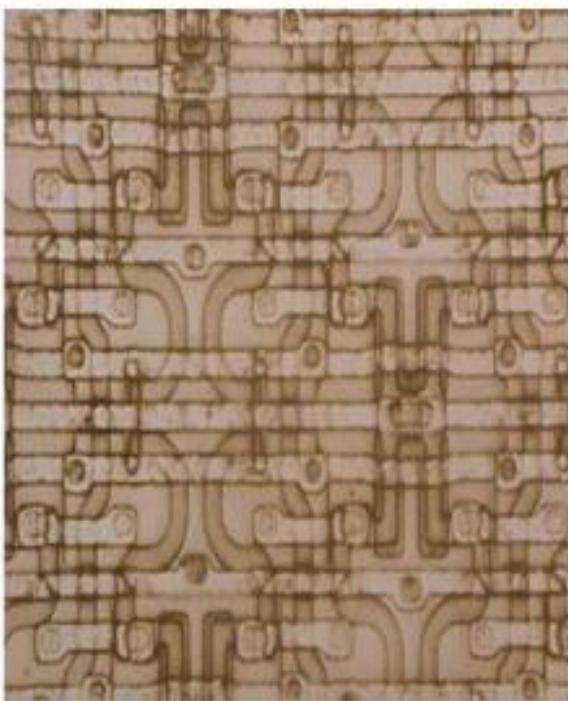
光を照射すると電流が流れる！

*Physics and  
Technology of  
Semiconductor  
Devices*  
by A.S. Grove

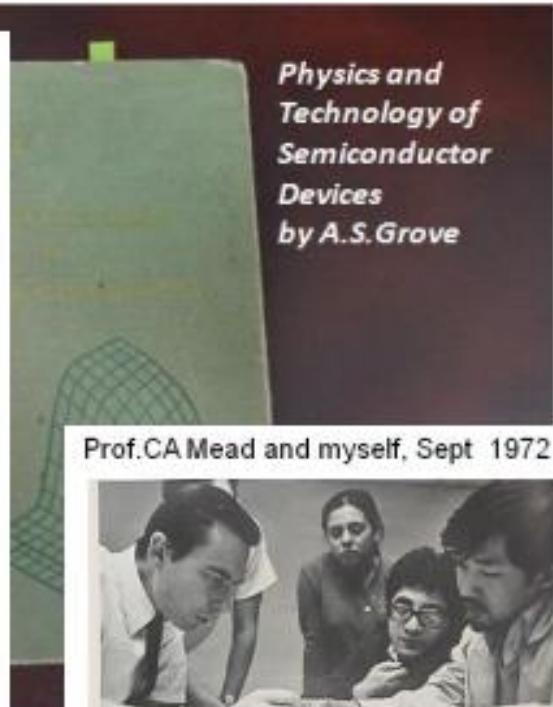
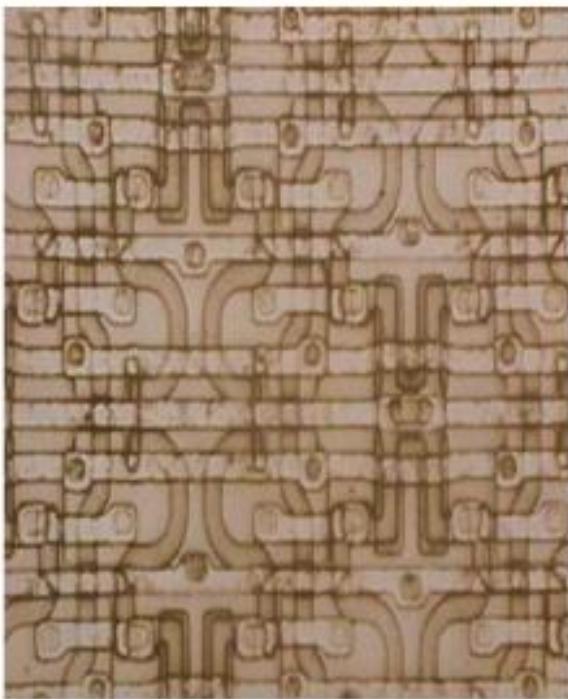


Prof. James McCaldin





1971 Intel 1101 256bit RAM



Prof.C.A Mead and myself, Sept 1972



1971 Intel 1101 256bit RAM

128 bit data comparator chip designed by CalTech and fabricated in Intel, 1972.

## 128-Bit Multicomparator

CARVER A. MEAD, RICHARD D. PASHLEY, MEMBER, IEEE, LEE D. BRITTON, YOSHIAKI T. DAIMON,  
AND STEWART F. SANDO, JR., MEMBER, IEEE

**Abstract**—A 128-bit multicomparator was designed to perform the search-test function on arbitrary length data strings. Device can be cascaded for longer block lengths or parallelized for bit-parallel, word-serial applications. The circuit utilizes a 3-phase static-dynamic shift register cell for data handling and a unique gated exclusive-or circuit to accomplish the compare function. The compare operation is performed bit parallel between a "data" register and a "key" register with a third "mask" register containing don't care bits that disable the comparison. The multicomparator was fabricated using p-channel silicon-gate metal-oxide-semiconductor (MOS) technology on a 107 × 150 mil chip containing 3350 devices. With transistor-transistor logic (TTL) input, data rates in excess of 2 MHz have been attained. The average power dissipation was 250 mW in the dynamic mode and 300 mW in the static mode.

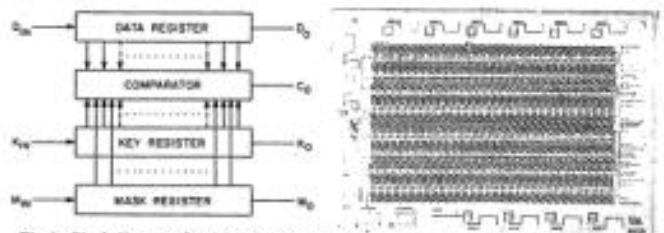
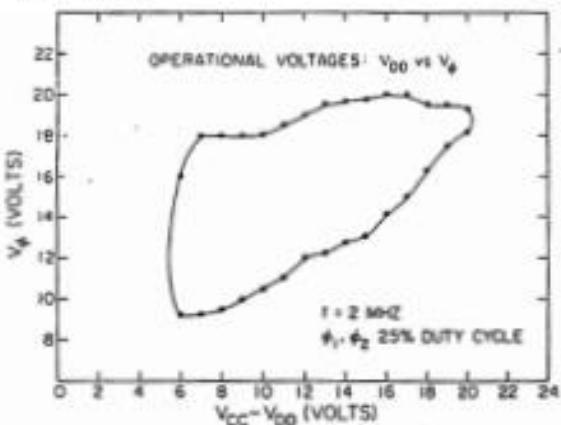
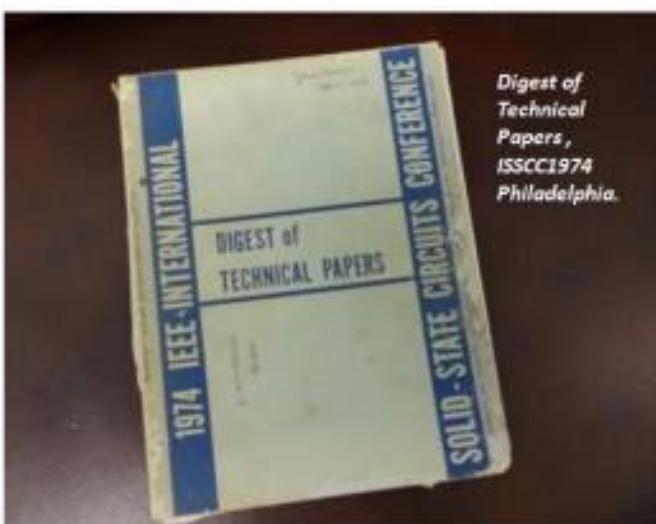


Fig. 1. Block diagram of multicomparator.



Prof. CA Mead and myself, Sept 1972



## Charge-Coupled Devices and Applications

Chairman

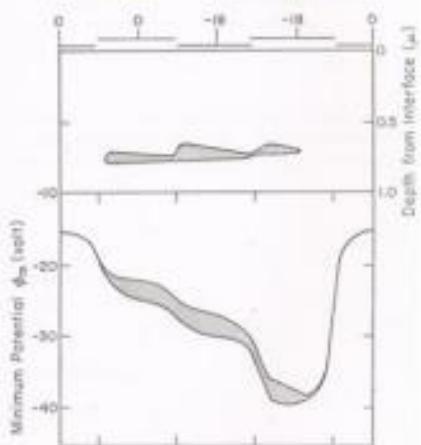
Lewis M. Terman

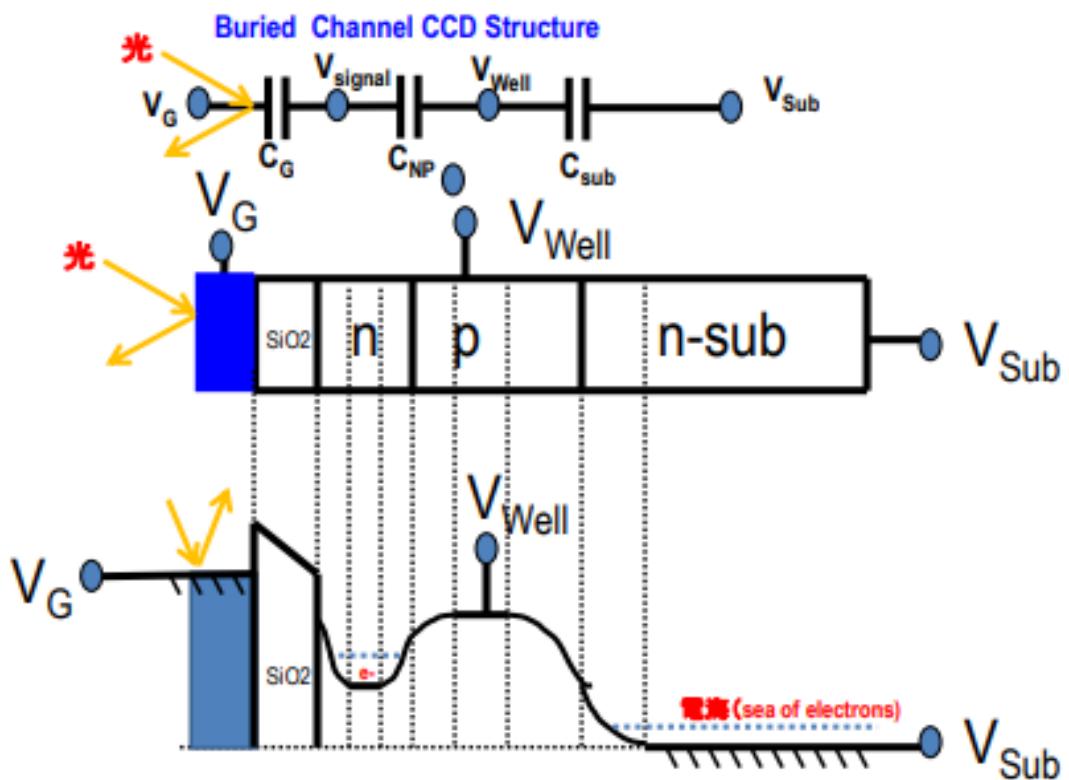
Testimony to the importance of the charge transfer phenomenon is attributed to the Morris R. Liebmann and the David A. Sarnoff awards this year to the originators of the charge-coupled and buried-channel devices, respectively. The papers in this session concentrate on the former.

## ISSCC1974 PhD Student Paper on buried channel CCD

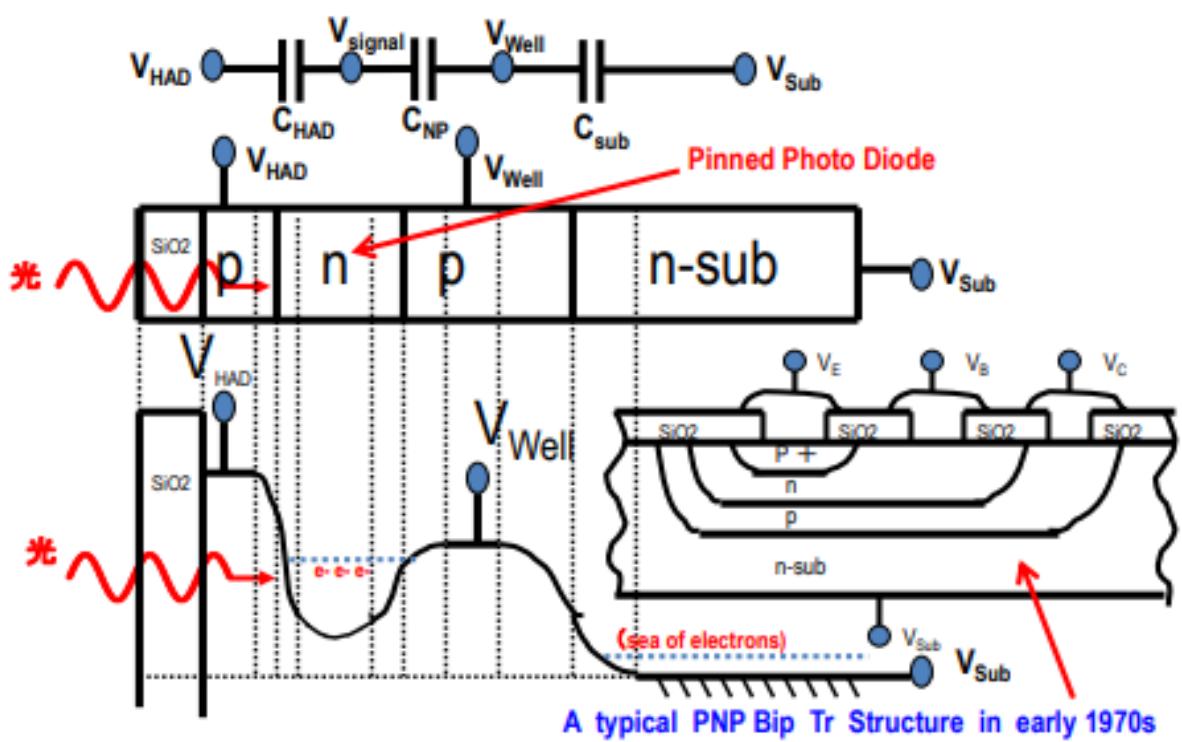


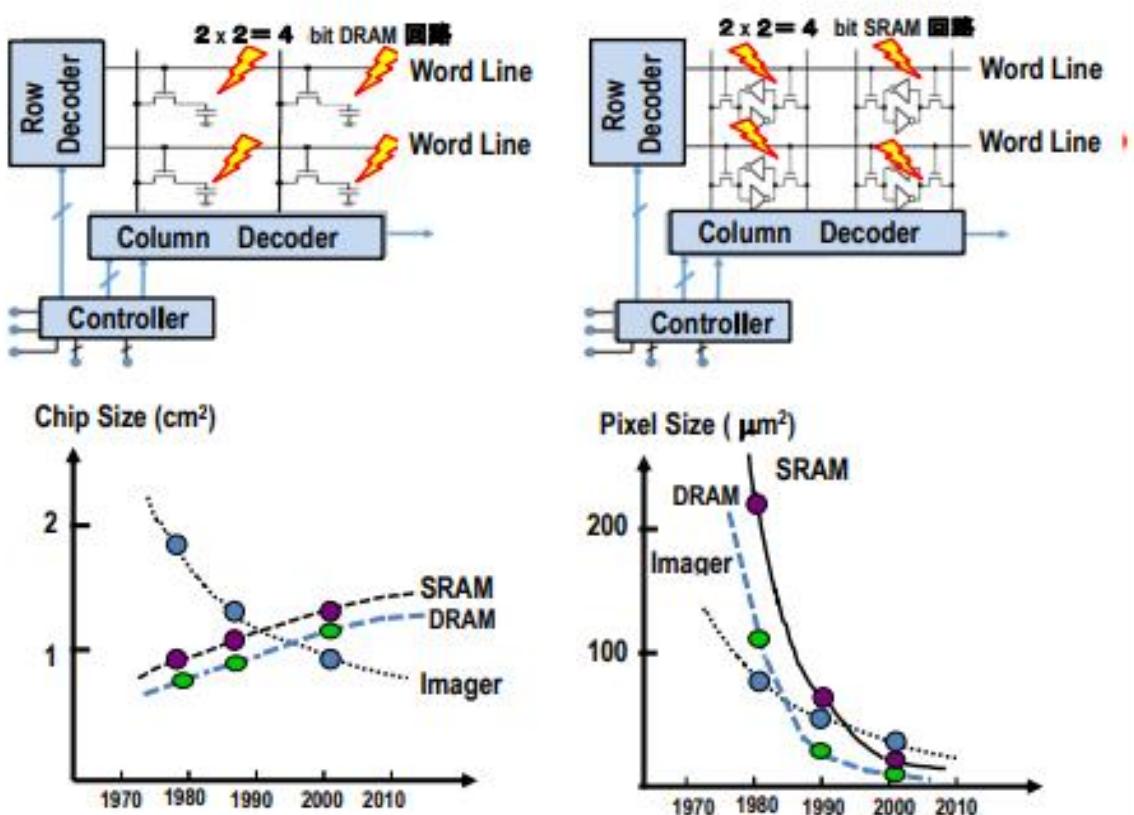
Prof. T. C. McGill





HAD ( hole accumulated diode ) sensor





XC-1 1980  
Two-Chip Color Video Camera



<ICX008>  
2/3 Inch 120K Pixel  
IT CCD Imager designed



1975-1982 Engineer in CCD Imagers and Camera System  
 1983-1989 Engineering Manager in SRAM/DRAM/ADC  
 1990-1998 General manager in Sony /NVM/MCU/PS1  
 1998-2008 Executive Staff Sony Semiconductor  
 Strategic Planning PS2/PS3



## IEEE Computer Elements Workshop @ Vail, Colorado, 1995



06

モンスター級の処理能力を発揮  
「CELLプラットフォーム」

**PS3**  
PlayStation-3

この電子部品の中身  
Hardwareを調査研究:  
Computer の構造とその  
アーキテクチャーを学ぶ。

比較対象: 2005年モデルPS3  
問題点と改良点に  
についてまとめる。

Cell B.E. 90nm, 65nm, 45nm

	90nm	65nm	45nm
Area	215.49mm <sup>2</sup>	109.00mm <sup>2</sup>	74.25mm <sup>2</sup>
W	11.7mm	11.25mm	6.47mm
H	19.25mm	11.25mm	6.47mm
SPE	14.5mm <sup>2</sup>	26.5mm <sup>2</sup>	14.5mm <sup>2</sup>
PPE	26.5mm <sup>2</sup>	-	-

West Cell B.E.

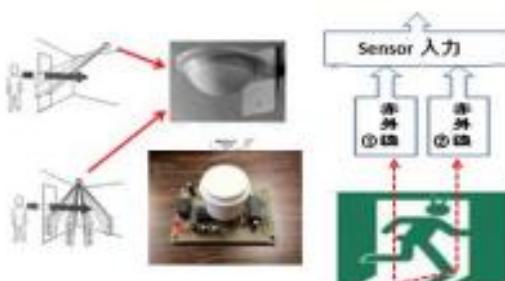
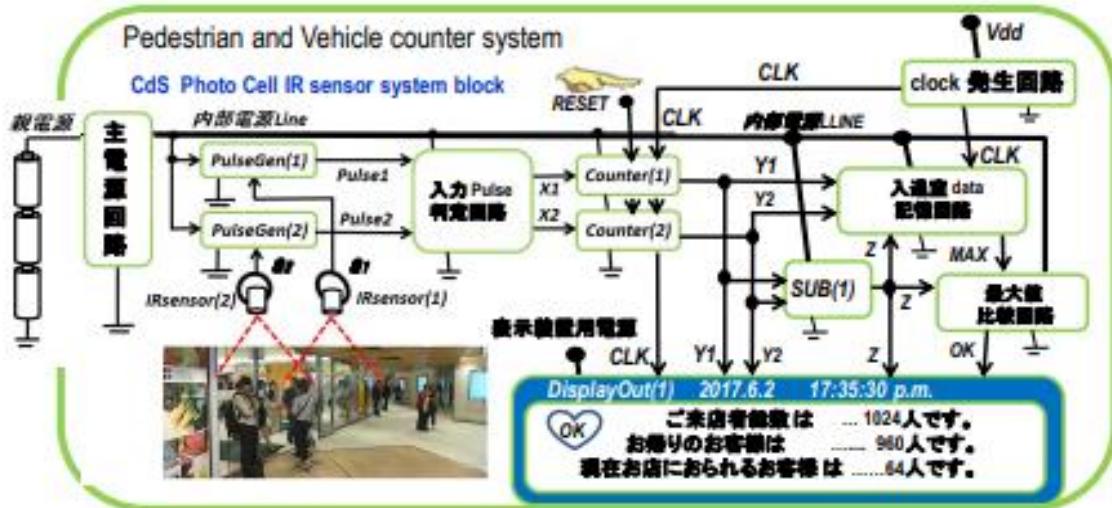
West Cell B.E.  
Area: 215.49mm<sup>2</sup>  
109.00mm<sup>2</sup>  
74.25mm<sup>2</sup>  
SPE: 14.5mm<sup>2</sup>  
PPE: 26.5mm<sup>2</sup>

East Cell B.E.

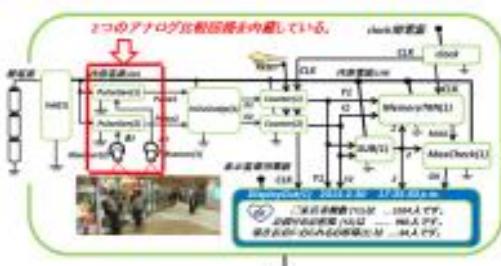
East Cell B.E.  
Area: 114.61mm<sup>2</sup>  
74.25mm<sup>2</sup>  
39.75mm<sup>2</sup>  
SPE: 11.5mm<sup>2</sup>  
PPE: 19.6mm<sup>2</sup>

Bottom Cell B.E.

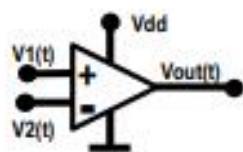
Bottom Cell B.E.  
Area: 115.49mm<sup>2</sup>  
49%  
W: 32.75mm  
H: 9.05mm  
SPE: 6.47mm<sup>2</sup>  
PPE: 11.52mm<sup>2</sup>



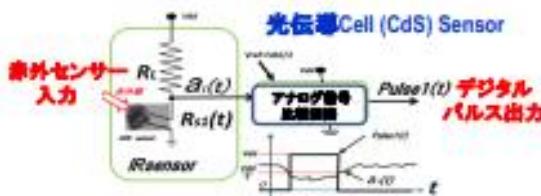
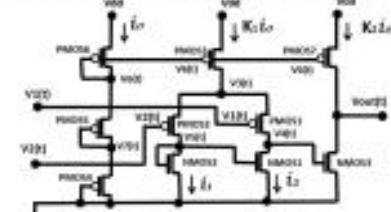
## 光伝導Cell (CdS) Sensor System 例



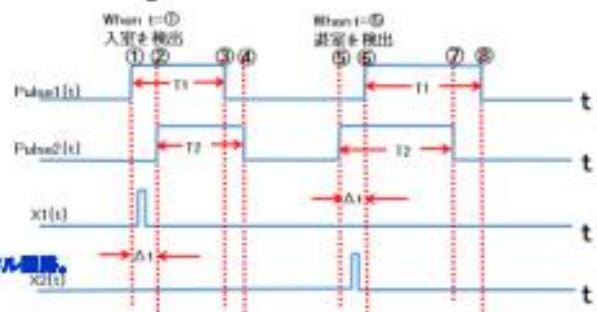
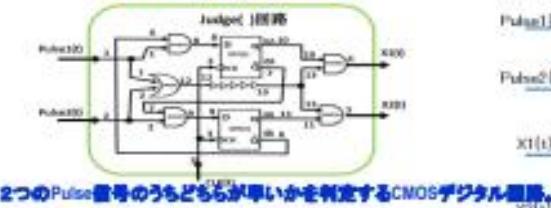
## アナログ信号比較回路（単純な 1 bit の A/D変換器）

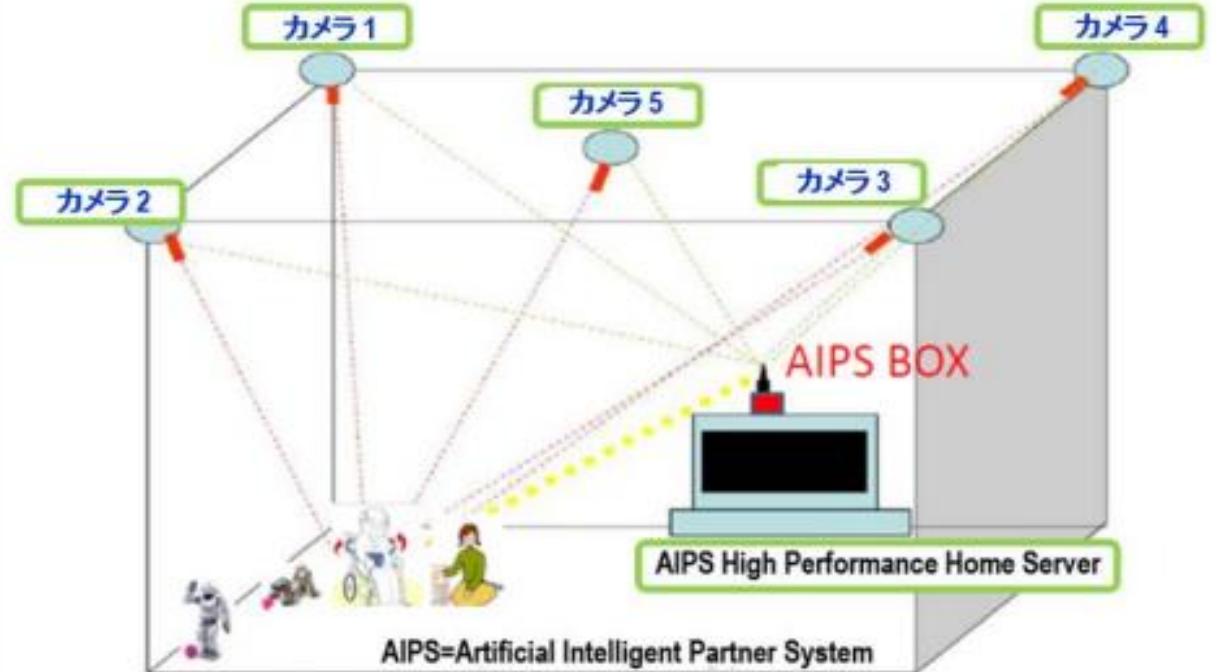
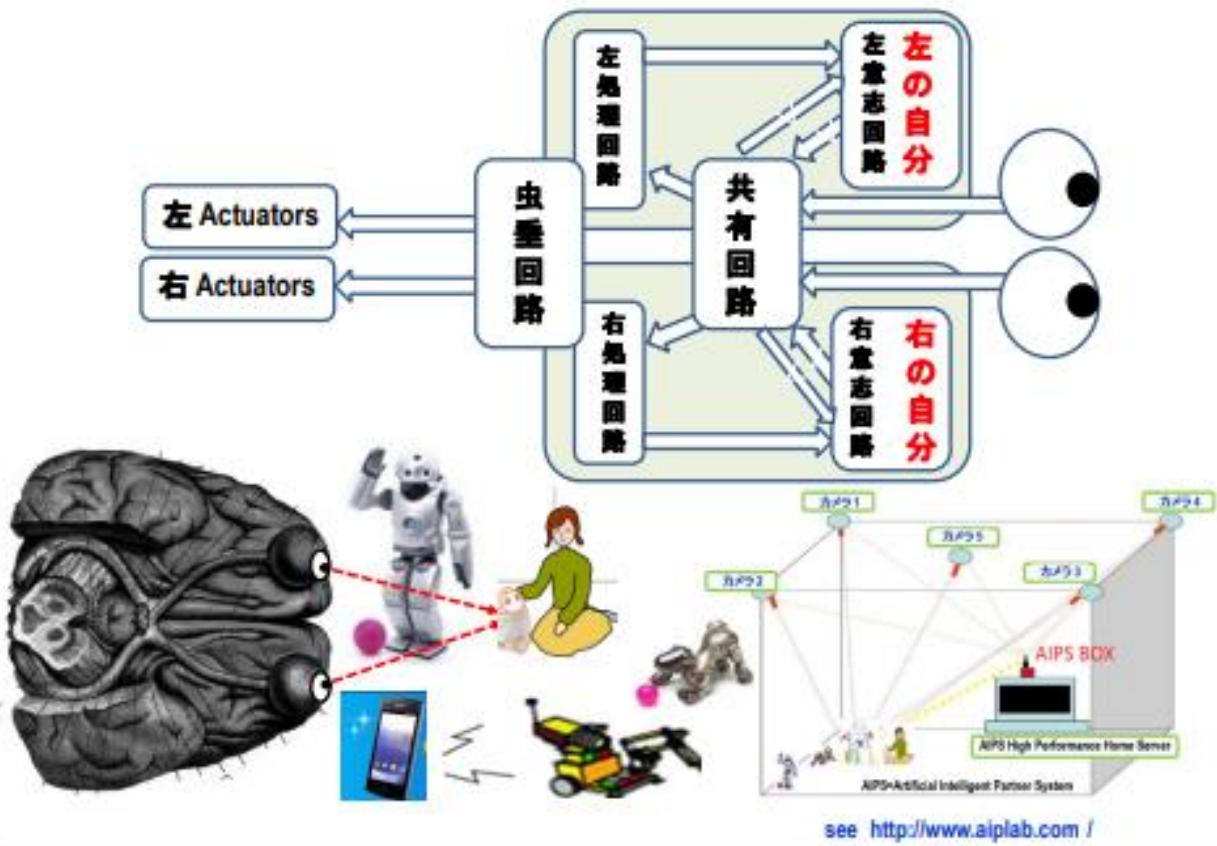


CMOS回路で構成されたアナログ信号比較回路



## 相対Pulse遅延判定回路





# 2017\_CoolChips\_Panel\_170419

2013年3月25日 午後4時  
フジテレビ全国NETで放送

